Interfacing the LTC1091 to the 8051 MCU

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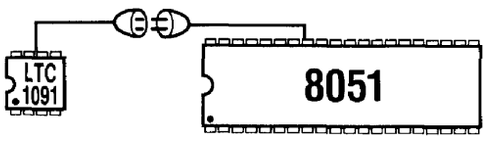

Introduction

This application note describes the hardware and software required for communication between the LTC1091 10-bit data acquisition system and the MCS-51 family of microcontrollers (e.g., 8051). The three wire interface is capable of completing a 10-bit conversion and transferring the data to the 8051 in 57μs. Configuration of the 8051 and the LTC1091 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be discussed. Finally, a summary of results including data throughput rates will be provided.

Interface Details

The serial port of the 8051 does not support the synchronous, half duplex format used by the LTC1091. Therefore it is necessary for the user to construct a serial port using three lines from one of the parallel ports available on the 8051. The lines are set or cleared using the bit manipulation features of the 8051. This provides a very flexible serial port.

The data lines (D_{IN} and D_{OUT}) of the LTC1091 can be tied together as shown in Figure 1. This can be done because the I/O pins on the 8051 can be configured as either inputs or outputs independently of one another during the data transfer.

Hardware Description

The 8051 was simulated and the code for this interface was developed on an Intel ICE252 emulator.

Due to the weak pullups of the 8051, excess loading should be avoided when examining the output of the microcontroller.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer. The 8051 clock rate was 2MHz. The clock could be run as high as 12MHz yielding the minimum conversion and transfer time of 57μs.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

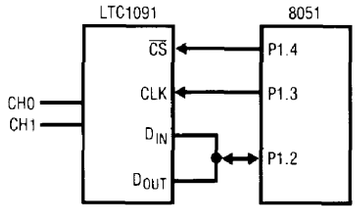

Figure 1. Schematic

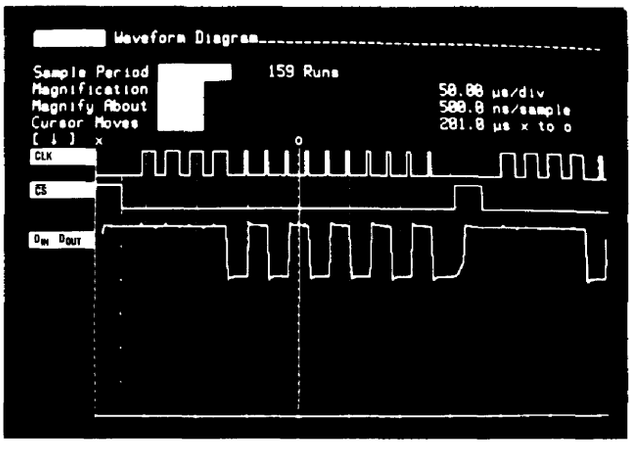

Figure 2. Timing Diagram

Software Description

The software simulates a serial port through bit manipulation instructions of the 8051.

$\overline{CS}$ is initialized by setting it high. Next the D_{IN} word for the LTC1091 is loaded into the accumulator. The LTC1091 is configured for MSB first and CH1 with respect to ground. Note that only the first four most significant bits of the byte loaded into the accumulator are sent to the LTC1091. The four LSBs of the D_{IN} word are don't cares.

$\overline{CS}$ is then cleared and a counter is set to four (the number of bits in the D_{IN} word). For each of the four D_{IN} bits the accumulator is shifted left with the MSB going into the carry bit. SCLK is cleared. The carry bit is output to D_{IN} and SCLK is set. The counter is decremented and checked and if all four bits have been output, P1.2 (D_{IN} and D_{OUT}) is set. This allows the pin to be used as an input now, to read the data in from the LTC1091.

SCLK is then cleared and the counter is set to nine (the first bit shifted out from the LTC1091 is a dummy, so nine shifts are required to fill the first byte.). The eight MSBs are read in the same manner as the D_{IN} word was output. The eight MSBs are stored in R2 and the remaining two LSBs are read into the accumulator. The LSBs are shifted into the MSBs of the accumulator and the remainder of the accumulator is masked to zeroes. The LSBs are then stored in R3 as shown in Figure 4. $\overline{CS}$ is then set and the process is completed. At this point the data is left justified.

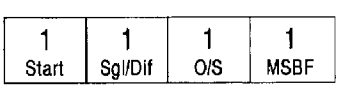

Figure 3. D_{IN} Word for LTC1091

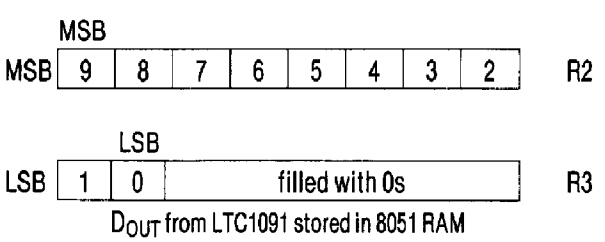

Figure 4. Memory Map

LABEL	MNEMONIC		COMMENTS
BEGIN	SETB	P1.4	$\overline{CS}$ GOES HIGH
AGAIN	MOV	A, #FFH	D_{IN} WORD FOR LTC1091
	CLR	P1.4	$\overline{CS}$ GOES LOW
	MOV	R4, #04H	LOAD COUNTER
LOOP1	RLC	A	ROTATE D_{IN} BIT INTO CARRY
	CLR	P1.3	SCLK GOES LOW
	MOV	P1.2, C	OUTPUT D_{IN} BIT TO LTC1091
	SETB	P1.3	SCLK GOES HIGH
	DJNZ	R4, LOOP 1	NEXT BIT
	MOV	P1, #04H	BIT 2 BECOMES AN INPUT
	CLR	P1.3	SCLK GOES LOW
	MOV	R4, #09H	LOAD COUNTER
LOOP	MOV	C, P1.2	READ DATA BIT INTO CARRY
	RLC	A	ROTATE DATA BIT INTO CARRY
	SETB	P1.3	SCLK GOES HIGH
	CLR	P1.3	SCLK GOES LOW
	DJNZ	R4, LOOP	NEXT BIT
	MOV	R2, A	STORE MSBs IN R2
	MOV	C, P1.2	READ DATA BIT INTO CARRY
	SETB	P1.3	SCLK GOES HIGH
	CLR	P1.3	SCLK GOES LOW
	CLR	A	CLEAR ACC
	RLC	A	ROTATE DATA BIT TO ACC
	MOV	C, P1.2	READ DATA BIT INTO CARRY
	RRC	A	ROTATE RIGHT INTO ACC
	RRC	A	ROTATE RIGHT INTO ACC
	ANL	A, #C0H	MASK UNUSED BITS
	MOV	R3, A	STORE LSBs IN R3
	SETB	P1.4	$\overline{CS}$ GOES HIGH

Figure 5. Code

Summary

A three wire interface between the LTC1091 and the 8051 with a combined data conversion and transfer time of 57μs was demonstrated. The data is transferred MSB first and resides in two bytes of the 8051 RAM in a left justified format. The code shown applies to all MCS-51 family members. The same technique can be used on any parallel port processor which allows individual bits to be programmed as inputs or outputs.